No new matter has been added, and the changes were made to facilitate clarification and ease of examination.

Examiner is encouraged to call the undersigned counsel to in order to resolve this matter.

Respectfully submitted,

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ADDENDUM TO PRELIMINARY AMENDMENT

Version with Markings to Indicate Changes Made

On page 3, beginning at line 26, please amend the paragraph as follows:

Figures [5] 5a and 5b [is] are [a] detailed diagrams of one embodiment of the linked list buffer monitor;

On page 3, beginning at line 28, please amend the paragraph as follows:

Figures [6] 6a and 6b show[s] one embodiment of a general linked list buffer monitor of the present invention;

On page 4, beginning at line 1, please amend the paragraph as follows:

Figures [7] 7a, 7b, 7c and 7d illustrate[s] one embodiment of an insert state machine of one embodiment of the present invention; and

On page 4, beginning at line 3, please amend the paragraph as follows:

Figures [8] 8a, 8b, 8c and 8d illustrate[s] one embodiment of a cell extraction state machine.

On page 10, beginning at line 21, please amend the paragraph as follows:

Referring to Figures [5] 5a and 5b, a detailed diagram of one embodiment of the linked list buffer monitor 212 is described. The link list monitor 212 includes up/down counter circuits that have adjustable counting thresholds. The first and second state machines that control the insert and extract logic, respectively, also control the linked list monitor. The insert logic state machine is used to increment the counters and the extract logic state machine is used to decrement the counters. Thus, the counters keep track of the size of each linked list contained in the buffer 230.

On page 13, beginning at line 5, please amend the paragraph as follows:

Referring to Figures [6] 6a and 6b, one embodiment of a general linked list buffer monitor 214 of the present invention is described in greater detail. The general monitor circuit includes three nine-bit counters 410(1) to 410(3). One counter 410(3) monitors the total cells in the buffer, both CBR and UBR. Again, the buffer can store up to 512 cells. A second one of the counters 410(1) monitors the total UBR cells in the buffer, and the third counter 410(2) monitors the total CBR cells in the buffer. Each counter has two programmable threshold levels.

On page 14, beginning at line 9, please amend the paragraph as follows:

The insert state machine 224 controls the flow of ATM cells from the LVDS ports to the linked list buffer. Referring to Figures [7] 7a, 7b, 7c and 7d, one embodiment of the insert state machine 224 is described. The insert state machine includes a list address circuit 500. The list address circuit includes sixteen nine-bit last pointers 510(1)-510(16)and multiplex circuitry that indicate the location of the last inserted cell in the linked list. One of the last pointers is used to point to the next cell location of a linked list. The cell data received by the data in circuitry 520 and the linked list address 530 are stored in the buffer. If a received cell is dumped from the LVDS, the insert operation is not performed. The cell is dumped if: the buffer is full (512 cells); the linked list has an overflow threshold violation; there is a total UBR overflow threshold violation and the incoming cell is not a delay priority cell; there is a total CBR overflow threshold violation and the incoming cell is a delay priority cell; there is a total buffer CLP threshold violation and the incoming cell is a less priority cell; there is a CLP threshold violation for a current linked list and the incoming cell is a less priority cell; there is a UBR CLP threshold violation and the incoming cell is a less priority cell and not a delay priority cell; and there is a CBR CLP threshold violation and the incoming cell is a less priority cell and a delay priority cell.

On page 14, beginning at line 26, please amend the paragraph as follows:

The cell extraction state machine 236 of one embodiment is described with reference to Figures [8] 8a, 8b, 8c and 8d. In one embodiment, the state machine

includes address decode circuitry 560 to determine the address of the next cell in a linked list. As explained above, the extract state machine updates the counters in the monitors when a cell is extracted from the buffer.